A CT Delta-Sigma Modulator for Wideband Applications

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ABSTRACT

This paper summarizes a 3rd order five bit continuous-time (CT) delta sigma modulator that obtains an ENOB of 10.77 for a signal bandwidth of 156 MHz .With some of the feedforward channels, the modulator structure is cascading of integrator with multiple feedback. The modulator also implements special path to reduce distortion inside the loop filter. The modulator signal transfer function (STF) and noise transfer function (NTF) are examined. The modulator coefficients are derived from discrete-time modeling, and feedback and feedforward coefficient are changed into continuous time coefficient. The feedback digital to analog (DAC) of pulse NRZ also included to cater stability of the modulator. The loop filter consists of integrator, which is implemented using operational amplifier. The DC gain of the operational amplifier is set to 75 dB considering for wideband application. The circuit in-idealities like jitter and input noise, DAC mismatch also simulated. The modulator also implements ELD compensation loop for the stability of the modulator.The modulator is evaluated with all circuitry non-idealities, and the result reveals that theattain signal to noise ratio of 66.66 dB, total harmonic distortion (THD) of 92 dB, signal to spurious free dynamic range (SFDR) of 88 dB for signal bandwidth of 156MHz with oversampling ratio of 16 having sampling frequency of 5 GHz.

Keywords:Bulk-driven amplifier, Analogtodigital converter, Digitaltoanalog converter, Noise transfer function, Signal Transfer Function

1. INTRODUCTION

For a signal bandwidth of 156 MHz, a 3rd order five-bitCT delta sigma modulator with an effective number of bit (ENOB) of 10.77 bit was produced. The modulator topology is cascade of integrator with multiple feedback (CIFB) for higher stability with some of the feedforward paths.A DT and CT delta sigma modulator design at transistor level in this paper.A high speed and high resolution ADC converter was created by combining a Continous time 1st stage and a Discrete time 2nd stage (ADC). The gain coefficients of Continuous time integrators in a feedforward scheme are improved to minimize power consumption of the CT first stage. Furthermore, in second stage integrators, double sampling (CDS) was used to further minimze power consumption. For such a 10 MHz signal bandwidth, the present new SDM is modeled in 180nm CMOS technology and obtains an 84 dB dynamic range. The measured total analogue power loss was 44 mW[1].This study focuses on design of wideband lowpower CT delta sigma modulator. To accomplish low power loop filter and cancel out of band peaking in (STF), aimproved feed forward architecture is provided. The circuits employ a variety of low-power, high speed design methods. Within a 20 MHz signal bandwidth, the modulator obtains 60 dB dynamic range (DR) at 25MHz signal bandwidth while achieved DR is 55dB.The power supply is 1.8 volt and current consumption is only 10mA when clocked at 400 MHz[2].The building

of a continuous time delta sigma for use in an ultrasound beamformer for biomedical imaging is presented in this paper. To increase resolution, modulator work at 1.2GHz. It replaces active adder in front of internal quantizer with a digital excessive loop delay (ELD) compensate. A delay-free feedback path is achieved by combining a digital control reference switching matrix with dataweighted averaging method. To ensure low clock jitter sensitivity and greater loop filter linearity, a multi-bit FIR feedback digital to analog converter and associated compensation circuit are used.This modulator attain dynamic range of 77.3dB while SNDR is 74.3dB and SNR is 77.3dB at signal bandwidth of 15MHz. The core modulator, which is made in 65 nm CMOS process, takes up only 0.16 mm^2 and consumption of power is 6.96 mWwhile supply voltage is 1 V. A merit figure of 58.6 fJ/conv. step is reached [3].High jitter robustness and low integrator dynamics, as well as superior linearity, can be accomplished in a singlebit continuous time delta sigma modulator by adjusting a finite impulse response filter in feedback digital to analog converter, according to recent state of theart designs digital to analog convertor.When usedtoContinoustime incrementally delta sigma modulators, however, the output of each and every FIR tap is irrelevant to input signal after every periodic resets of the loop-filter, and it takes some time to return to normal operations. This causes substantial swing overshoot at the integrator outputs in the beginning portion of each incrementally conversion cycle, limiting the modulator's dynamic range (DR) and so negating the advantages of FIR DAC. The difficulties of attaining a FIR DAC in an incrementally modulator are described in this paper. In addition, two design strategies are demonstrated for mitigating swing overshoots and achieving normal modulator action. This permits for a greater number of FIR taps to be employed in an incrementally delta sigma modulator modulator, which is advantageous for high-speed/high-resolution systems [4].

This paper proposeda wideband noise shaping delta-sigma modulator for signal bandwidth of 100 MHz. The proposed modulator loop filter is fifth order, while the quantizer is a 4-bit. The modulator investigated for topologies CIFB and CIFF. Both modulators utilize out-of-band gainof 4 and oversampling ratio of 16 and can attain signal to noise ratio of 108 dB. The CIFF topology signal transfer function peaking compared to CIFB topology of CIFB. The NTF of the modulator shows the accurate noise shaping considering ideal operational amplifier in the integrators. The modulator also implements NTF zero optimizations method to minimize further in band quantization noise. The DC gain causes reduction of resolution of the modulator, so maximum DC gain amplifier are used in the integrator. Limited slew-rate issues for all the integrators are discussed. The circuit non-idealities like thermal noise and flicker noise also simulated at MATLAB. An extra amplifier for the CIFF topology also discussed and trade-off for the higher performance of the modulator. The CIFB topology provides higher stability for the higher order of loop filter, so CIFB topology also considered. Therefore, the modeling and MATLAB simulation shows that the modulator can obtain SNR of 108 dB at oversampling ratio (OSR) of 16 with four-bit quantizer for signal bandwidth of 100 MHz.

After the introduction, the second section discuss the design of the modulator design with CIFB structure, while the third-order five-bit continuous-time third section describes the modeling and simulation of the modulator and explain the operational amplifier for integrator for the third-order 5-bit quantizerfor CT design implementation. Finally, the section four concludes the paper.

2. MODULATORDESIGN

A higher order with three integrators in the loopfilter and five-bit quantizer modulator modeled using Delta-Sigma Toolbox [12]. The CIFBinvestigated for higher out-of-band-gain(OBG) of 2 with moderate oversampling ratio of 16 without NTF zero optimization technique. The modulator with CIFB topology can achieve SNR of 68 dB with OSR of 16.Due to the reason of low pass modulator, the STF of modulator have low pass behavior. While the NTF have high pass response to shape more quantization noise at high frequency. The coefficients of the proposed 3rdorder multiple bit CIFB obtained from Delta-Sigma Toolbox.These coefficientsrepresent the ratio of capacitors at the discrete-time implementation of the modulator. While for the CT implementation these coefficient needs to be converted into the CT equivalent coefficient [13]. Then these converted coefficients will be used to choose the resistor and capacitor ratio considering the sampling frequency. Those coefficients which are not mentioned, have value zero.The STF and NTF of the modulator is shown in Figure 1. As it is shown from the Figure 1 clearly that the OBG of the CIFB modulator is 2. While STF of the modulator shows low-pass response to allow those signals, which are at low frequencies and attenuate high frequency signal. The

Figure 2 shows the STF and NT plot, due to CIFB topology the STF response is flat which shows no peaking effect. The Figure.3 shows the output power spectral density (PSD) plot with SNR of 68, achieving effective number of bit (ENOB) of 10-bit. The modulator NTF shows a sharp noise shaping response due to the reason that all integrator inside the loopfilter is assumed having infinite DC gain. The noise floor is at the level of -140dB, the quantization noise is suppressed maximum with nine

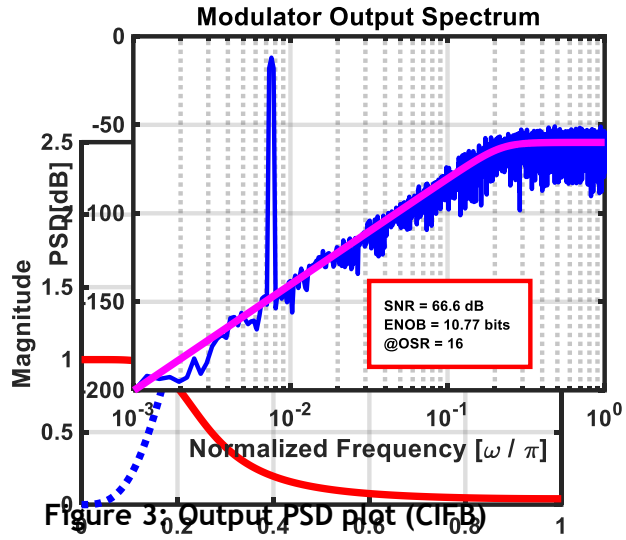

Figure 3: Output PSD plot (CIFB)

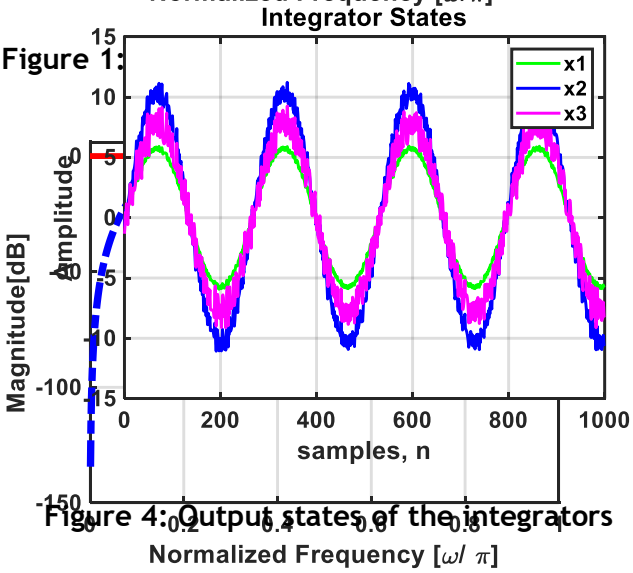

Figure 4: Output states of the integrators

Figure 1:

Figure 2: STF and NTF (CIFB)

integrators inside the loop filter.Due to

moderate OSR of 16, the signal bandwidth is high. Due to CIFB topology of the modulator the signal swing inside the loopfilter is large as a results operational amplifier with very high DC gain will be demanded for the suppression of the quantization noise. Due to CIFB topology the stability of the loopfilter is very high due to the advantage of multiple feedbacks, while the overall modulator becomes power hungry with many high DC gain amplifier inside the loopfilter.

3. RESULTS & DICUSSION

A third-order five-bit CT delta sigma modulator toachieve ENOB of 10.77 bit for signal bandwidth of 156 MHz. The modulator topology is cascade of integrator with multiple feedback with some of the feedforward paths. The modulator also implements special path to reduce distortion inside the loop filter. The simulation environment SDToolbox[14] which simulates the circuit non-idealities are used. This section will discuss about the circuit non-idealities like thermal noise or kT/C, flicker noise, finite operational amplifier gain, finite slew-rate, finite gain-bandwidth (GBW).

4. CONCLUSION

For a signal bandwidth of 156 MHz, a third-order five-bit CT delta sigma modulator with an effective number of bit (ENOB) of 10.77 bit was developed. The modulator topology is cascade of integrator with multiple feedback with some of the feedforward paths. The modulator also implements special path to reduce distortion inside the loop filter. The NTF and STF of the modulator are discussed. The modulator coefficients are derived from discrete-time modeling, and feedback and feedforward coefficient aretransformed into a constant time coefficient. The feedback digital to analog (DAC) of pulse NRZ also included to cater stability of the modulator. The loop filter consists of integrator, which is implemented using operational amplifier. The DC gain of the operational amplifier is set to 75 dB considering for wideband application. The circuit in-idealities like jitter and input noise, DAC mismatch also simulated. The modulator also implements ELD compensation loop for the stability of the modulator. The modulator with all circuit non-idealities is simulated and results show that modulator can obtain signal to noise ratio of 66.66 dB, total harmonic distortion (THD) of 92 dB, signal to spurious free dynamic range (SFDR) of 88 dB for signal bandwidth of 156MHz with oversampling ratio of 16 having sampling frequency of 5 GHz.

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